

KA-9640
PATENT APPLICATION

1017 U.S. PTO
10/083399
02/27/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Toshihiro TANAKA et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND A METHOD OF
TESTING THE SAME

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any
assertion as to materiality or prior art effect, the
document listed on the attached Form PTO-1449 is hereby
cited.

The document listed on the attached List is cited in
the specification, on pages 3 and 4, and its relevance is
indicated therein.

Respectfully submitted,

MWS:lmb

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February 27, 2002

FORM PTO-1449				Atty. Docket No. XA-9640		Appln. No.	
<u>LIST OF DOCUMENTS CITED BY APPLICANT</u>				Applicant Toshihiro TANAKA et al.			
				Filing Date HEREWITH		Group	

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U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AJ	5-265579	10/15/93	JAPAN			abstract
	AK						
	AL						
	AM						
	AN						
	AO						
OTHER (including author, title, date, pertinent pages, etc.)							
	AP						
	AQ						
	AR						
Examiner				Date Considered			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							